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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HARKNESS, CHARLES A	
ART UNIT	**PAPER NUMBER**
2183	2

DATE MAILED: 03/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/738,485	KORGER, PETER	
	Examiner	Art Unit	
	Charles A Harkness	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

2. The applicant or their representatives are urged to review the specification and submit corrections for all mistakes of a grammatical, clerical, or typographical nature.

Drawings

3. New corrected drawings are required in this application because Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Vegesna et al, U.S. Patent Number 5,226,142 (herein referred to as Vegesna).

5. Referring to claims 1 and 15 Vegesna has taught a circuit comprising:

a register stack configured as (i) a plurality of segments addressable through a segment address signal and (ii) a plurality of registers within each of said plurality of segments, said

plurality of registers being addressable through a register address signal (Vegesna figure 6, figure 8; in figure 8, the register address signal is line are 90, while the segment address signal is made up of the signals coming from the result vector driver 68 and of the 106, 108, 110, and 112); and

a control circuit configured to (i) store a plurality of register states (Vegesna figures 6 and 8 column 2 lines 14-25; there are both global and local and shared registers present, therefore the system would have to be able to distinguish between the different states), (ii) store a segment count signal (Vegesna column 3 lines 51-65; the pointer is incremented and decremented like a counter), and (iii) present said segment address signal responsive to said plurality of register states, said segment count signal, and said register address signal (Vegesna figure 8 numbers 90, 94, 98, 100, 68; the register address is fed in on line 90, the result vector driver 68 must keep track of which registers are in which states, so that it can determine which signals to operate and pass the data on, and the CWP, or window pointer then selects the 106 or 108 lines to turn on, in the case of a write to the registers).

6. Referring to claim 2 Vegesna has taught wherein at least one of said register states is fixed in a global state (Vegesna figure 6 and 8 column 2 lines 14-25).

7. Referring to claim 3 Vegesna has taught wherein at least one of said register states is fixed in a stackable state (Vegesna figure 6 and 8 column 2 lines 14-25).

8. Referring to claim 4 Vegesna has taught wherein said register stack further comprises:

a first portion configured as at least one segment of said plurality of segments; and

a second portion remote from said first portion and configured as at least one segment of said plurality of segments (Vegesna figure 6 and 8; different segments that do not touch each other are in the stack of registers).

9. Referring to claim 5 Vegesna has taught wherein said control circuit comprises:

a counter configured to present said segment count signal (Vegesna column 3 lines 51-65; the pointer is incremented and decremented like a counter);

a status circuit configured to present a gating signal responsive to said register address signal (Vegesna figure 8 result vector driver; the result vector driver takes in input from the register address and uses that to determine where the data should be directed to; the result vector driver is a logical device and thus made up of logic gates, and thus would have internal gating signals); and

a plurality of logic gates configured to present said segment address signal responsive to said gating signal and said segment count signal (Vegesna figure 8 the lines making up the segment address signal 106 and 108 come from logic derived from the CWP, window pointer, and the gating signals from the result vector driver would be passed out on the lines of 91, 93, 95, and 97 as the other part of the segment address signal).

10. Referring to claim 6 Vegesna has taught wherein said status circuit comprises:

a comparator configured to present said gating signal responsive to said plurality of register states and said register address signal (Vegesna figure 8 column line 43-column 11 line 6; since the result vector driver 68 must decide which type of register lines to send the result through to the register file, based upon the register lines, the result vector driver must have a knowledge of which type, or state, a register is based upon its address, therefore the register state information must be stored in the result vector driver, and must be compared to the register address; the gating signal is then outputted as part of the segment address signal to the register file).

11. Referring to claim 7 Vegesna has taught wherein said status circuit comprises:

a memory device configured to store said plurality of register states and present said gating signal responsive to said plurality of register states and said register address signal (Vegesna figure 8 column line 43-column 11 line 6; since the result vector driver 68 must decide which type of register lines to send the result through to the register file, based upon the register lines, the result vector driver must have a knowledge of which type, or state, a register is based upon its address, therefore the register state information must be stored in the result vector driver; the gating signal is then outputted as part of the segment address signal to the register file).

12. Referring to claim 8 Vegesna has taught wherein said plurality of logic gates are further configured to present said segment address as a predetermined address responsive to said gating signal having a global state (Vegesna figure 8 column line 43-column 11 line 6; since the result vector driver 68 must decide which type of register lines to send the result through to the register file, based upon the register lines, the result vector driver must have a knowledge of which type, or state, a register is based upon its address, therefore the register state information must be stored in the result vector driver; the gating signal is then outputted as part of the segment address signal to the register file based on the register state, or type being global, local, or shared).

13. Referring to claim 9 Vegesna has taught wherein said status circuit comprises:

a comparator configured to present said gating signal responsive to said plurality of register states and said register address signal (Vegesna figure 8 column line 43-column 11 line 6; since the result vector driver 68 must decide which type of register lines to send the result

through to the register file, based upon the register lines, the result vector driver must have a knowledge of which type, or state, a register is based upon its address, therefore the register state information must be stored in the result vector driver, and must be compared to the register address; the gating signal is then outputted as part of the segment address signal to the register file).

14. Referring to claim 10 Vegesna has taught a method of controlling a register stack comprising the steps of:

(A) comparing a register address with a plurality of register states to present a gating signal (Vegesna figure 8 column line 43-column 11 line 6; since the result vector driver 68 must decide which type of register lines to send the result through to the register file, based upon the register lines, the result vector driver must have a knowledge of which type, or state, a register is based upon its address, therefore the register state information must be stored in the result vector driver, and must be compared to the register address; the gating signal is then outputted as part of the segment address signal to the register file);

(B) gating a segment count with said gating signal to present a segment address (Vegesna column 3 lines 51-65; the pointer is incremented and decremented like a counter; figure 8 the lines making up the segment address signal 106 and 108 come from logic derived from the CWP, window pointer, and the gating signals from the result vector driver would be passed out on the lines of 91, 93, 95, and 97 as the other part of the segment address signal); and

(C) addressing said register stack with said register address and said segment address (Vegesna figure 8 numbers 90, 94, 98, 100, 68; the register address is fed in on line 90, which then drives the result vector driver 68 which sends out part of the segment address signal; and the

CWP, or window pointer then selects the 106 or 108 lines to turn on, in the case of a write to the registers for the other part of the segment address signal).

15. Referring to claim 11 Vegesna has taught wherein step (A) further comprises the sub-steps of:

presenting a signal communicating said plurality of register states; and

selecting one of said plurality of register states as said gating signal based upon said register address (Vegesna figure 8 column line 43-column 11 line 6; since the result vector driver 68 must decide which type of register lines to send the result through to the register file, based upon the register lines, the result vector driver must have a knowledge of which type, or state, a register is based upon its address, therefore the register state information must be stored in the result vector driver; the gating signal is then outputted as part of the segment address signal to the register file based on the register state, or type being global, local, or shared).

16. Referring to claim 12 Vegesna has taught further comprising the step of:

setting said plurality of register states in response to a reset handler operation (Vegesna figure 8 column line 43-column 11 line 6; since the result vector driver 68 must decide which type of register lines to send the result through to the register file, knowing whether the type is global, local, or shared; in addition, when everything is cleared, the states of the registers would have to be set at some point, so the result vector driver knows which state each register is).

17. Referring to claim 13 Vegesna has taught further comprising the step of:

incrementing said segment address in response to a push instruction (Vegesna column 7 lines 5-15; the CWP operates as the window counter and is incremented and decremented based on calls and returns from subroutines).

18. Referring to claim 14 Vegesna has taught further comprising the step of: decrementing said segment address in response to a pop instruction (Vegesna column 7 lines 5-15; the CWP operates as the window counter and is incremented and decremented based on calls and returns from subroutines).

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR 1.111(c).

Joy et al., U.S. Patent Number 5,083,263, has taught a system with register windowing in a ring structure that includes local and global registers and a window counter.

Stone et al., U.S. Patent Number 5,636,362 has taught a stack frame cache using second region as a storage if first region is full.

Fujii et al., U.S. Patent Number 5,437,043 has taught a register file that can be used both as scalar registers of a register window and as vector registers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579. The examiner can normally be reached on 8:00 A.M. – 5:30 P.M. with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-7579.

Charles Allen Harkness

Patent Examiner

Art Unit 2183

March 18, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100